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10EC45

Fourth Semester B.E. Degree Examination, June 2012
Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the structure of VHDL module and verilog module. **(06 Marks)**

b. Explain verilog data types. **(06 Marks)**

c. Discuss different logical operators used in HDLs. **(08 Marks)**

2 a. Explain the execution of signal assignment statement in HDL with example. **(06 Marks)**

b. Write VHDL code for 2×1 multiplexer with active low enable in data flow description. **(07 Marks)**

c. Write verilog code for 2×2 unsigned combinational array multiplier. **(07 Marks)**

3 a. With the suitable example, explain the case statement in both VHDL and verilog. **(06 Marks)**

b. Explain the flowchart of booth multiplier algorithm with example. Also write VHDL code for 4×4 bit booth algorithm. **(14 Marks)**

4 a. What is binding in VHDL? Explain.
i) Binding between entity and architecture in VHDL.
ii) Binding between entity and component in VHDL.
iii) Binding between library and module in VHDL. **(08 Marks)**

b. Write verilog structural description of full adder. Use this full adder to design 3-bit comparator and write the verilog structural code for the same. **(12 Marks)**

PART – B

5 a. Write HDL code for converting an unsigned binary to an integer using procedure and task. **(10 Marks)**

b. Explain built-in procedures for file-processing in VHDL. **(10 Marks)**

6 a. Why mixed type description needed? Explain. **(04 Marks)**

b. Write HDL code (both VHDL and verilog) for finding the greatest element of an array. **(12 Marks)**

c. Discuss VHDL package with example. **(04 Marks)**

7 a. How to invoke a VHDL entity from verilog module? Explain with an example. **(08 Marks)**

b. Write mixed language description of a 3-bit adder with zero flag. If the output of the adder is zero, the zero flag is set to 1; otherwise it is set to 0. **(12 Marks)**

8 a. Explain synthesis steps with flow chart. **(10 Marks)**

b. Find the gate level mapping for the following verilog code:

```
module if_st(a, y);
input [2 : 0] a;
output y ;
reg y ;
always @ (a)
begin
        if (a < 3′b101)
           y = 1′b1;
        else
           y = 1′b0;
end
end module
```

(06 Marks)

c. Discuss synthesis information extraction from entity in VHDL. **(04 Marks)**

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